

**REMARKS**

This is in response to the Office Action mailed on February 14, 2002.

Claims 1 through 13 are currently pending in the application.

As further discussed herein below, Applicant respectfully submits that the cited prior art does not support a *prima facie* case of obviousness. Therefore, reconsideration of the above-referenced application is respectfully requested.

**35 U.S.C. § 103(a) Obviousness Rejections**

**(A) Applicable Authority**

The basic requirements of a *prima facie* case of obviousness are summarized in MPEP §2143 through §2143.03, *i.e.*, in order “to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine the reference teachings. Second, there must be a reasonable expectation of success in combining the references. Third, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the expectation of success must both be found in the prior art, and not based on Applicants’ disclosure.” *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Further, in establishing a *prima facie* case of obviousness the initial burden is placed on the examiner. “To support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or impliedly suggest the claimed invention or the examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references.” *Ex parte Clapp*, 227 USPQ 972, 973 (Bd. Pat. App. & Inter. 1985). See also MPEP § 706.02(j) and § 2142.

The Supreme Court has established the standard of patentability to be applied in obviousness rejections in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966). This standard has been summarized in MPEP § 2141 into four factual inquires including “(A)

**Serial No. 09/921,423**

determining of the scope and contents of the prior art; (B) ascertaining the differences between the prior art and the claims in issue; (C) resolving the level of ordinary skill in the pertinent art; and (D) evaluating evidence of secondary considerations." It should be noted that, when applying the required patentability standards of *Graham*, the basic considerations which apply to obviousness rejections based on 35 U.S.C. § 103 should include the following principles of patent law: "(A) the claimed invention must be considered as a whole; (B) the references must be considered as a whole and must suggest the desirability and thus the obviousness of making the combination; (C) the references must be viewed without the benefit of impermissible hindsight vision afforded by the claimed invention; and (D) reasonable expectation of success is the standard with which obviousness is determined." *Hodosh v. Block Drug Co., Inc.*, 786 F.2d 1136, 1143 n.5, 229 USPQ 182, 187 n.5 (Fed. Cir. 1986).

**(B) Obviousness Rejection Based on Hsia et al. (U.S. Patent 5,827,783) in view of Wolf et al. (ISBN 0-9616721-6-1) and Haller et al. (U.S. Patent 5,804,506)**

Claims 1 through 9, 10, and 13 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Hsia et al. (U.S. Patent 5,827,783, hereinafter "Hsia") in view of Wolf et al. (ISBN 0-9616721-6-1, hereinafter "Wolf") and Haller et al. (U.S. Patent 5,804,506, hereinafter "Haller").

Hsia generally relates to a stacked capacitor in a memory device formed adjacent to a shallow trench isolation and more particularly, relates to a stacked capacitor in a high density memory device formed adjacent to a shallow trench isolation wherein the capacitor has a corrugated side-wall structure (Hsia, col. 1, lines 5-12). The corrugated side-wall structure is obtained by depositing a plurality of oxide layers by a deposition method alternating between a thermal CVD method and a plasma CVD method for each of the layers and etching them to form a capacitor cell contact in a contact etch process by using a plasma etching technique. Polysilicon and dielectric layers are then deposited in the capacitor cell to form the capacitor (*Id.*, col. 3, lines 1-16). Hsia does not teach or disclose doping the different layers to alter the etching rates of the

**Serial No. 09/921,423**

different layers. In fact, Hsia specifically teaches that the different etching rates are a result of the "different densities of the oxide layers formed by the thermal CVD method and by the plasma CVD method and their different etch selectivity to an acid-based etchant such as hydrogen fluoride" (*Id.*, col. 6, lines 10-19). Hsia also discloses that "the etch selectivity of the oxide layers can also be controlled by the processing parameters used in the deposition process. For instance, the gap (or the electrode spacing), the reactant gas pressure and the plasma power level can influence the properties of the oxide film obtained and consequently, its etch selectivity" (*Id.*, col. 6, lines 29-34). Disclosure made by Hsia to other etchants refer specifically to the use of different acid etchants rather than the use of doping agents in the different layers to be etched, e.g., "it should be noted that hydrofluoric acid is illustrated as one example of the wet etchant that has the proper selectivity between the oxide layers prepared by the different techniques. Other etchants that perform similarly with suitable selectivity between the oxide layers may also be used to achieve the same desirable result achieved by hydrogen fluoride" (*Id.*, col. 7, lines 7-12).

Wolf's book publication teaches that borophosphosilicate glass or BPSG finds wide use as the pre-metal dielectric layer between polysilicon and metal and dielectrics between stacked capacitors and metal in DRAMs (Wolf, page 200, lines 3-5).

Haller discloses a method of fabricating an integrated circuit on a semiconductor substrate including the steps of forming a tungsten silicide conductor structure having a nitride encapsulating layer on the substrate and disposing a doped nonconducting layer over the conductor structure. A self-aligned contact etch is performed wherein the etch is a selective etch of the conductor structure and the nonconducting layer. The selective etch preferentially removes material forming the nonconducting layer rather than material forming the conductor structure. The nonconducting layer is preferably doped with germanium. A germanium concentration of 5% to 25% in the nonconducting layer provides the preferred increased selectivity of the etch (Haller, col. 2, lines 55-67, emphasis added). Applicant kindly submits that Haller does not teach or disclose the use or selective etching of adjacent single layers or a plurality of layers of alternating or non-alternating non-conductive materials, including BPSG and germanium-doped BPSG.

Based on the teachings and disclosures of the references cited and summarized hereinabove, Applicant respectfully submits that Hsia, Wolf, and Haller, either individually or in any combination thereof, do not support a *prima facie* case of obviousness under 35 U.S.C. § 103 of

**Serial No. 09/921,423**

the present invention recited in independent claims 1 through 9 because, at the very least, there is no suggestion or motivation to modify the references or to combine the reference teachings. In response to the statement that "it would have been obvious to one of ordinary skill in the art to modify the invention by Hsia et al ... as to select boro-phospho silicate glass... and germanium boro-phospho silicate glass" (Office Action, page 4, lines 11-15), the Office is kindly reminded that "a statement that modifications of the prior art to meet the claimed invention would have been well within the ordinary skill of the art at the time the claimed invention was made because the references relied upon teach that aspects of the claimed invention were individually known in the art is not sufficient to establish a *prima facie* case of obviousness without some objective reason to combine the teachings of the references. *Ex parte Levengood*, 28 USPQ2d 1300 (Bd. Pat. App. & Inter. 1993). See also *In re Kotzab*, 217 F.3d 1365, 1371, 55 USPQ2d 1313, 1318 (Fed. Cir. 2000). See also *In re Rouffet*, 149 F.3d 1350, 1357, 47 USPQ2d 1453, 1457-58 (Fed. Cir. 1998) (The combination of the references taught every element of the claimed invention, however without a motivation to combine, a rejection based on a *prima facie* case of obvious was held improper.). The evidentiary showing of a motivation or suggestion to combine prior art references "must be clear and particular." *In re Dembiczaik*, 175 F.3d 994, 999, 50 U.S.P.Q.2d 1614, 1617 (Fed. Cir. 1999).

In the present instance, there has been no objective reason set forth for any proposed combination of the cited prior art. As noted in the Office Action (e.g., Office Action, page 4, lines 1-3), nowhere in Hsia's patent one finds any teaching or disclosure of the use of germanium doping of the selective layers to produce the desired selective etching effects. Hsia only teaches selective etching of a plurality of different non-conductive layers based on the effect that distinct etchants have thereon due to the variation in densities thereof resulting from the different vapor deposition methods used to create the different layers, i.e., thermal or plasma CVD. Variations on the etching methods taught only included alterations in processing parameters (such as electrode spacing, the reactant gas pressure and the plasma power level) or the use of different etchants. As documented supra, *Hodosh*, the patentability standard for a case of obviousness requires that a reference be considered as a whole. "Portions arguing

**Serial No. 09/921,423**

against or teaching away from the claimed invention must be considered." *Bausch & Lomb, Inc. v. BarnesHind/Hydrocurve, Inc.*, 230 USPQ 416 (Fed. Cir. 1986). Therefore Applicant respectfully submits that Hsia, when considered as a whole, teaches away from the use of doping to produce the resultant selective etching of the different layers. "A *prima facie* case of obviousness may also be rebutted by showing that the art, in any material respect, teaches away from the claimed invention." *In re Geisler*, 116 F.3d 1465, 1471, 43 USPQ2d 1362, 1366 (Fed. Cir. 1997). See also M.P.E.P. §2145(X)(D)(2) (citing *In re Grasselli*, 713 F.2d 731, 743, 218 U.S.P.Q. 769, 779 (Fed. Cir. 1983) "it is improper to combine references where the references teach away from their combination.").

Furthermore, although Wolf discloses that non-conductive borophosphosilicate glass or BSPG finds wide use as the pre-metal dielectric layer between polysilicon and metal, and dielectrics between stacked capacitors and metal in DRAMs, it does not teach the use of germanium doping. The Office cites Haller in support of the use of germanium doping even though Haller does not disclose or teach the use of different non-conductive layers—it dopes only a single, non-conductive layer so as to effect a faster etching rate thereof in comparison with a conductive tungsten silicide conductor structure having a nitride encapsulating layer. Applicant respectfully submits that the desirability of such combination has not been documented to set forth any objective reason for such a combination. "The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination." *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990). See also *In re Fritch*, 972 F.2d 1260, 23 USPQ2d 1780 (Fed. Cir. 1992) (holding that "although a prior art device may be capable of being modified to run the way the apparatus is claimed, there must be a suggestion or motivation in the reference to do so."). Therefore, Applicant respectfully submits that only the use of impermissible hindsight based on the subject matter recited in the above-referenced application justifies the proposed combination or modification of Hsia, Wolf, and Haller. However, "it is impermissible to use the claimed invention as an instruction manual or 'template' to piece together the teaching of the prior art so that the claimed invention is rendered obvious . . . . One cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention." *In re Fritch*, 23 U.S.P.Q.2d 1780 (Fed. Cir. 1992).

Claims 10 and 13 are allowable, among other reasons, as depending either directly or indirectly from claim 9, which is allowable.

Additionally, the finding of obviousness of claim 10 based on Official Notice that "it is obvious [to have] one dielectric layer and a conductive layer over said at least one dielectric layer in the art of capacitors generally and in the art of semiconductor memory device capacitors in particular, in the sense that otherwise one would not have a capacitor" (Office Action, page 14, lines 2-6)) is respectfully objected to. This objection is grounded on the fact that such an action is contrary to the required patentability standards of *Graham*, *supra*, and principles of patent law requiring that, when a determination of obviousness is made, "the claimed invention must be considered as a whole." *Hodosh*, *supra*. The Office is respectfully reminded that in establishing the differences between the prior art and a claimed invention "the question under 35 U.S.C. § 103 is not whether [a particular manufacturing method or process conventionally practiced in a industry] would have been obvious, but whether the claimed invention as a whole would have been obvious." *Stratoflex, Inc. v. Aeroquip Corp.*, 713 F.2d 1530, 218 USPQ 871 (Fed. Cir. 1983); *Schenck v. Nortron Corp.*, 713 F.2d 782, 218 USPQ 698 (Fed. Cir. 1983). In particular, when the subject matter recited in claim 10 is considered as a whole, it is apparent that a capacitor cell having a portion thereof formed by a plurality of layers of boro-phospho silicate glass and a plurality of layers of germanium boro-phospho silicate glass, each layer of germanium boro-phospho silicate glass having at least a portion thereof contacting at least a portion of at least one layer of said plurality of layers of boro-phospho silicate glass and at least one dielectric layer and a conductive layer over said at least one dielectric layer has neither been taught nor disclosed in the cited prior art references.

Applicants request the citation of specific prior art to illustrate such a proposition.

Therefore, for the above-discussed reasons, Applicant respectfully requests withdrawal of the obviousness rejections under 35 U.S.C. § 103 of claims 1 through 9, 10, and 13.

(C) Obviousness Rejection Based on Hsia, Wolf and Haller (U.S. Patent 5,804,506) as applied to claim 10 above, and further in view of Kawakubo (U.S. Patent 5,889,696).

Claim 11 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Hsia, Wolf and Haller as applied to claim 10 above, and further in view of Kawakubo et al (U.S. Patent 5,889,696, hereinafter "Kawakubo").

Kawakubo relates to a semiconductor memory device arranging a plurality of memory cells in a matrix format, each of which includes a thin-film capacitor having a ferroelectric film and a pair of electrodes facing each other via the ferroelectric film, and a transfer gate transistor connected to the thin film capacitor (Kawakubo, abstract, lines 1-6). Kawakubo discloses the use of barium strontium titanate (BST) for the ferroelectric film (*Id.*, col. 2, lines 29-34) because of its large effective relative dielectric constant resulting in high charge storage ability and a relatively stable dielectric constant (*Id.*, col. 9, lines 58-63). Kawakubo does not suggest or teach the use of tantalum pentoxide ( $Ta_2O_5$ ) and silicon nitride ( $Si_3N_4$ ) as dielectric elements or the use of doping to effect selective etching of different layers of non-conductive materials. In fact, Kawakubo uses the same selective etching using hydrofluoride acid disclosed by Hsia (*Id.*, col. 9, lines 28-38).

Applicant respectfully reasserts that Hsia, Wolf, and Haller, individually or in any combination thereof, do not support a *prima facie* case of obviousness under 35 U.S.C. § 103 of the present invention recited in independent claim 9 because there is no suggestion or motivation to modify the references or to combine the reference teachings as discussed hereinabove. The addition of Kawakubo's teachings to the combination of Hsia, Wolf, and Haller does not remedy the teaching-away argument presented hereinabove as applied to Hsia thus the lack of motivation to combine the references or teachings found therein remains. The Office cites Kawakubo in support of the use of BST as a high dielectric element (one of the three dielectric substances recited in claim 11). Although not explicitly stated in the Office Action, Applicant assumes that the Derwent Information Summary of the U.S. Patent to Deboer et al (summarized herein below as related to the rejection of claim 12) is the art teaching and disclosing the other two dielectric elements recited in claim 11, i.e., tantalum pentoxide ( $Ta_2O_5$ ) and silicon nitride ( $Si_3N_4$ ). With the lack of motivation to combine the cited references, this piece-by-piece combination of prior art to

Serial No. 09/921,423

teach isolated features recited in the instant invention can only be explained by impressive hindsight use thereof. Applicant respectfully submits that claim 11 is allowable, among other reasons, as depending either directly or indirectly from claim 9, which is, as discussed hereinabove, allowable. Therefore, Applicant respectfully requests withdrawal of the obviousness rejections under 35 U.S.C. § 103 of claim 11.

(D) Obviousness Rejection Based on Hsia, Wolf and Haller as applied to claim 10 above, and further in view of DeBoer et al. (U.S. Patent 5,930,106 and Derwent copy, under "Novelty").

Claim 12 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Hsia, Wolf and Haller as applied to claim 10 above, and further in view of DeBoer et al. (U.S. Patent 5,930,106, hereinafter "DeBoer" and the Derwent Information Summary, under "Novelty," hereinafter "Derwent").

Deboer relates to the use of the new ability to form thin films of tantalum pentoxide and silicon nitride with electrode-limited conduction and consistent film thickness and dielectric properties. This dielectric layer is used in combination with a silicon-germanium charge storage electrode to give a highly reliable storage capacitor (Derwent, novelty summary). The capacitor comprises first and second plates sandwiching a dielectric layer of preferably tantalum pentoxide or silicon nitride or their combination or barium titanate, which is dominated by electrode-limited conduction. At least one of the electrode plates comprises a silicon-germanium layer as its charging surface (*Id.*, detailed description). In particular, Deboer teaches only capacitors having single layers of a conductive electrode 21, a dielectric layer 31, and a top capacitor electrode or plate 41 (Deboer, col. 3, lines 24-28 and Fig. 4).

Similarly as discussed above in Subsection (C), Applicant respectfully reasserts that Hsia, Wolf, and Haller, individually or in any combination thereof, do not support a *prima facie* case of obviousness under 35 U.S.C. § 103 of the present invention recited in independent claim 9 because there is no suggestion or motivation to modify the references or to combine the reference teachings

**Serial No. 09/921,423**

as discussed hereinabove. The addition of Deboer's teachings to the combination of Hsia, Wolf, and Haller does not remedy the teaching-away argument presented hereinabove as applied to Hsia thus the lack of motivation to combine the references or teachings found therein remains. Further, as recited in claim 9 of the present invention, Applicant respectfully submit that Deboer does not teach "a capacitor cell having a portion thereof formed by a plurality of layers of boro-phospho silicate glass and a plurality of layers of germanium boro-phospho silicate glass, each layer of germanium boro-phospho silicate glass having at least a portion thereof contacting at least a portion of at least one layer of said plurality of layers of boro-phospho silicate glass" (emphasis added). Deboer is cited to support a finding of obviousness of the use of silicon-germanium as a conductive layer as recited in claim 12. Additionally, as already discussed in Subsection (C) it is implied in the Office Action that Deboer is also cited in support of the two dielectric elements recited in claim 11, i.e., tantalum pentoxide ( $Ta_2O_5$ ) and silicon nitride ( $Si_3N_4$ ). Again, with the lack of motivation to combine the cited references, the use of the present invention as template to find support in the related art to teach isolated features recited in the instant invention can only be explained by impressive hindsight use thereof. Applicant respectfully submits that claim 12 is allowable, among other reasons, as depending either directly or indirectly from claim 9, which is, as discussed hereinabove, allowable. Therefore, Applicant respectfully requests withdrawal of the obviousness rejections under 35 U.S.C. § 103 of claim 12.

Serial No. 09/921,423

### CONCLUSION

Claims 1 through 13 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicants' undersigned attorney.

Respectfully submitted,



James R. Duzan  
Attorney for Applicants  
Registration No. 28,393  
TRASKBRITT, PC  
P.O. Box 2550  
Salt Lake City, Utah 84110  
(801) 532-1922

Date: April 15, 2002

JRD/sls:djp

N:\2269\3978.1\Amendment 3-22-02.doc